

ABSTRACT

A method and apparatus are described for operating a first processor connected with a first bus in an active mode so that the first processor controls the first bus, operating a second processor
5 connected with a second bus in an active mode so that the second processor controls the second bus, detecting faults via hardware associated with the first processor and the second processor, and responsive to an occurrence of a fault in the first processor, transferring control of the first bus to the second processor via hardware associated with the first processor and the second processor.

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